REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

The Applicants appreciate the allowance of claims 4 and 5.

By the foregoing amendment claim 3 has been amended. Claim 1 has been previously canceled without prejudice or disclaimer for filing in a continuation application. Thus, claims 2-14 are currently pending in the application and subject to examination. No new matter has been added, as the subject matter of the amendment to claim 3 may be found in the application as filed at, for example, page 5, lines 17-19.

Rejection Under 35 U.S.C. § 103(a)

In the outstanding Office Action dated May 2, 2008, claims 2-3 and 8-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malcolm, U.S. Patent No. 6,373,954 (hereinafter, "Malcolm") in view of Tsukamoto et al., U.S. Patent No. 4,815,352 (hereinafter, "Tsukamoto") and Inoue et al., U.S. Patent No. 5,532,765 (hereinafter, "Inoue"). Claims 6-7 were rejected Under 35 U.S.C. § 103(a) as being unpatentable over Malcolm as modified by Tsukamoto and Inoue as applied to claim 1 above, and further in view of Anderson, U.S. Patent No. 6,078,594 (hereinafter, "Anderson"). It is noted that claim 1 has been previously canceled, and claim 3 has been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

In the Applicant's invention as recited in independent claim 3, as amended, the digital/analog converting means is structured by a plurality of digital/analog converters and the digital/analog converters are in cascade connection. Further, the cascade

connection is a connection in which an output of each of the digital/analog converters is connected to another one of the digital/analog converters as a reference voltage.

By the claimed invention, if the D/A converters are cascade-connected to each other, it is possible to reduce the number of bits of each converter, and thus, to greatly reduce the area needed for the D/A converter. For example, by the claimed invention, if a 16-bit D/A converter is required, two 8-bit D/A converters may be cascade-connected to construct the 16-bit converter. In such a case, the area for the 8-bit D/A converter becomes 1/256 of the area for the 16-bit D/A converter, and therefore, even if two 8-bit converters are needed, the area is 2/256 of the 16-bit converter. As explained below, none of the applied art of record, alone or combined, teaches or suggests at least the features of the claimed invention noted above, and therefore, also do not provide the advantages made attainable by the claimed invention.

Inoue

The outstanding Office Action asserts that Inoue discloses in Figure 19 and at col. 14, lines 22-67, thereof, that Inoue discloses a digital/analog converting means structured by a plurality of digital/analog converters and the digital/analog converters are in cascade connection.

Figure 19 of Inoue appears to show that the output of the D/A is connected to the input of the succeeding D/A as if a cascade connection is made. However, as disclosed at col. 14, lines 58-60 of Inoue, the respective D/As of Figure 19 receive the output signal from the serial data producing circuit 27. The output of the D/A is not connected to the input of the succeeding D/A. The outputs of the D/As are connected to the inverted amplifying circuit 40. In Inoue, the address included in the output signal of the

circuit 27 indicates any one of the D/As 28-39 which fetch the data (as shown in Figure 21A) output from the serial data producing circuit 27 in accordance with the address and the other output signal of the circuit 27 (as shown in Figures 21B and 21C and described as col. 14, lines 45-57). Thus, what are fetched by the respective D/As are not the output of the preceding D/A but the output of the serial data producing circuit 27.

Furthermore, in Inoue, the waveform data from the correction waveform generating circuit 25 is input to the reference of each D/A, not the output of the preceding D/A.

As described above, although it appears as if the D/As are cascaded-connected in Figure 19 of Inoue, it is abundantly clear from the description of Inoue that these D/As 28-39 are not cascade-connected, as are the digital/analog converters of the claimed invention.

Furthermore, Inoue relates to an image correction apparatus, and especially, a correction waveform generating circuit 42 relating to convergence correction. The field of art of Inoue is entirely different from that of the claimed invention. Accordingly, Inoue fails to teach or suggest the audio processing and the PCM of the claimed invention. Tsukamoto, Malcolm and Anderson are not cited for, nor do they cure the deficiencies of Inoue explained above.

Tsukamoto

Moreover, in Applicant's invention as recited in independent claim 3, as amended, includes M sets (M being a natural number) of independent digital/analog converting means for converting digital data over a sound channel into an analog sound signal; data output control means for controlling an output of data to said digital/analog

converting means; and time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction; whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N...

With particular respect to Tuskamoto, three channels shown in Figure 17 of Tuskamoto are indicative of the physical channels because the number of the digital/analog converters is three and, thus, the number of the speakers is also three. That is, the physical channels are equal to the monaural channel in Figure 1 and the stereo channels in Figure 2 of the subject application. The sound channels of the claimed invention are not physical channels, and indicate the logical channels. Therefore, in the claimed invention, the logical channels of N*M are assigned to a single physical channel, as is clearly indicated in Figures 1 and 2 of the subject application. Accordingly, the claimed invention is entirely different from that which is disclosed by Tsukamoto.

Further, In Tsukamoto, one D/A is allotted to one physical channel. In contrast, in the present invention, M sets of D/As are assigned to one physical channel, and each of the M sets of D/As receives the data of the N sets of sound channels (logical channels) being time-division-multiplexed. Therefore, in the present invention, to one physical channel, N*M logical sound channels are assigned.

Furthermore, in Tsukamoto, the multiplexer allots the plurality of slots being time-divided-multiplexed on any one of the three physical channels. In contrast, there is no means in the present invention for allotting the data of N*M sound channels (logical

channels), and the data of all N*M sound channels (logical channels) is applied to one physical channel.

An advantage of having M sets of D/As as recited in the claimed invention is described in the instant application, at, for example, Figure 5 in which four (4) sets of D/As are provided, and each of them receives the signal that the data of four channels are multiplexed.

If only one set of D/A and to which the signal that the data of sixteen (16) channels are multiplexed is applied, it is necessary to reproduce the 16 channels during one period shown in Figure 5, the effective period of each channel (the period except the no Sound period) becomes short, the efficiency of the D/A becomes bad, and the sound quality is affected. However, by providing the 4 sets of D/As (as shown in the example), the effective period of each channel is prolonged and thus, the efficiency of the D/A can be increased.

Tsukamoto further shows that three D/As are not cascade-connected, and only receive the input signal form the dc-multiplexer.

Accordingly, Tsukamoto fails to disclose or suggest at least the features of M sets (M being a natural number) of independent digital/analog converting means for converting digital data over a sound channel into an analog sound signal; data output control means for controlling an output of data to said digital/analog converting means; and time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction; whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a

product of M and N, wherein said digital/analog converting means is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection, said cascade connection being a connection that an output of each of said digital/analog converters is connected to another one of said digital/analog converters as a reference voltage, as recited in independent claim 3, as amended.

For all of the reasons explained above, it is clear that Tsukamoto fails to teach or remotely suggest the presently claimed invention.

Inoue, Malcolm and Anderson are not cited for, nor do they cure the deficiencies of Tsukamoto explained above.

As explained above, none of the applied art of record, nor any combination therefore, discloses or suggests each and every feature recited in independent claim 3, as amended.

For at least this reason, the Applicant submits that claim 3 is allowable over the applied art of record. As claim 3 is allowable, the Applicant submits that claims 2 and 5-14, which depend from allowable claim 3, are likewise allowable for at least the reasons set forth above with respect to claim 3.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 2-14 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100341-00003.

Respectfully submitted,

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